

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
7 October 2004 (07.10.2004)

PCT

(10) International Publication Number
WO 2004/085717 A1

(51) International Patent Classification⁷: **C30B 25/02,**
H01L 21/205

(21) International Application Number:
PCT/EP2003/003136

(22) International Filing Date: 26 March 2003 (26.03.2003)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US): **EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH [CH/CH];** Rämistrasse 101, CH-8092 Zürich (CH).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **VON KAENEL, Hans** [CH/CH]; Eigenheimstrasse 3, CH-8304 Wallisellen (CH).

(74) Agent: **HEUSCH, Christian;** OK pat AG, Chamerstrasse 50, CH-6300 Zug (CH).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

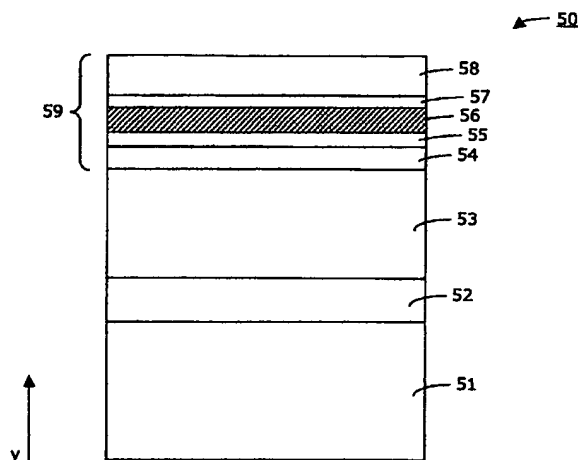
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FORMATION OF THIN SEMICONDUCTOR LAYERS BY LOW-ENERGY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION AND SEMICONDUCTOR HETEROSTRUCTURE DEVICES



(57) Abstract: Method for forming a highly relaxed epitaxial semiconductor layer (52) with a thickness between 100nm and 800nm in a growth chamber. The method comprises the steps: - providing a substrate (51) in the growth chamber on a substrate carrier, - maintaining a constant substrate temperature (T_s) of the substrate (51) in a range between 350°C and 500°C, - establishing a high-density, low-energy plasma in the growth chamber such that the substrate (51) is being exposed to the plasma, - directing Silane gas (SiH_4) and Germane gas (GeH_4) through the gas inlet into the growth chamber, the flow rates of the Silane gas and the Germane gas being adjusted in order to form said semiconductor layer (52) by means of vapor deposition with a growth rate in a range between 1 and 10 nm/s, said semiconductor layer (52) having a Germanium concentration x in a range between $0 < x < 50\%$.

WO 2004/085717 A1